Replaced by Article 34

10/518740

CLAIMS

1. A phase-locked loop comprising:

a voltage controlled oscillator for generating an output signal and having a frequency control input for controlling the frequency of the output signal, and

a phase comparator for deriving a control signal from a phase error detected in response to the received output signal and a reference signal, said control signal being coupled to the frequency control input of said voltage controlled oscillator, wherein the phase comparator includes:

a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in the reference signal,

a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in the received output signal, and

means or arithmetic means for determining the phase error from the obtained first and second accumulated phase values.

2. A phase-locked loop according to claim 1, further comprising a divider for dividing the frequency of the output signal, whereby the received output signal received by the phase comparator is a frequency-divided output signal.

3. A phase-locked loop according to claim 1 or 2, wherein the arithmetic means are subtracting means for determining the phase error by a subtraction between the obtained first and second accumulated phase values.

4. A phase-locked loop according to claim 3, wherein the subtracting means are adapted for subtracting the second accumulated phase value from the first accumulated phase value.

5. A phase-locked loop according to any one of the claims 1-4, wherein the phase comparator includes a digital-to-analogue converter adapted to convert the phase error and thereby to generate an analogue output signal.

6. A phase-locked loop according to any one of the claims 1-4, wherein the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for generating a first analogue representation of said first logic bit by bit AND operation, and

means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND operation.

7. A phase-locked loop according to claim 6, wherein the converter circuit comprises current mode logic circuits giving a current output for a two input AND operation, said current output being used for generating an analogue representation for a bit by bit AND operation.

8. A phase-locked loop according to claim 6 or 7, wherein the arithmetic means are adapted to obtain one or more analogue phase error signals based on the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

9. A phase-locked loop according to claim 8, wherein the arithmetic means comprises subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the first analogue representation.

10. A phase-locked loop according to any one of the claims 1-5, wherein the phase comparator includes a first and a second digital-to-analogue converter adapted to convert the first and the second accumulated phase value and thereby to generate analogue representations thereof, and that the arithmetic means are adapted to perform an analogue subtraction of the analogue representation of the second accumulated phase value from the analogue representation of the first accumulated phase value.

11. A phase-locked loop according to claim 10, wherein the phase comparator includes a first and a second AND-means, where the output of said first AND-means is connected to the first digital-to-analogue converter, whereby the first accumulator is connected to a first non-inverting input of said first AND-means and whereby the second accumulator is connected to a first inverting input of said first AND-means, the output of said second AND-means being connected to said second digital-to-analogue converter, and that said second accumulator further is connected to a first non-inverting input of said second AND-means, said first accumulator further being connected to a first inverting input of said second AND-means.

12. A phase-locked loop according to any one of the claims 1-11, wherein the phase comparator includes a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator, and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

13. A method for determining a phase error in response to a first signal and a second signal, said method comprising the steps of:

generating a first reoccurring trigger event in response to the first signal,

generating a second reoccurring trigger event in response to the second signal,

incrementing a first phase value by a first predetermined increment value when the first trigger event occurs to obtain a first accumulated phase value,

incrementing a second phase value by a second predetermined increment value when the second trigger event occurs to obtain a second accumulated phase value, and

calculating or determining said phase error based on obtained first and second accumulated phase values.

14. A method according to claim 13, said method comprising the step of frequency dividing the first signal and/or the second signal, whereby the generation of the first and/or second reoccurring trigger event is performed in response to the frequency divided first and/or second signal, respectively.

15. A method according to claim 13 and 14, wherein the calculation of the phase error is based on a subtraction of said second accumulated phase value from said first accumulated phase value.

16. A method according to any one of the claims 13-15, wherein the first accumulated phase value, the second accumulated phase value and the phase error are represented by binary numbers.

17. A method according to any one of the claims 13-15, wherein the first accumulated phase value and the second accumulated phase value are represented by binary numbers and the phase error is represented by an analogue signal.

18. A method according to claim 17, said method further comprising the steps of:

performing a first logic bit by bit AND operation of the first accumulated phase value and the inverted second accumulated phase value, and generating a first analogue representation of said first logic bit by bit AND operation, and

performing a second logic bit by bit AND operation of the second accumulated phase value and the inverted first accumulated phase value, and generating a second analogue representation of said second logic bit by bit AND operation.

19. A method according to claim 18, wherein the calculation of the phase error comprises generating one or more analogue phase error signal based on the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

20. A method according to claim 19, wherein the calculation of the phase error comprises performing an analogue subtraction of the second analogue representation from the first analogue representation.

21. A method according to any one of the claims 16-20, wherein the most significant bit of the first accumulated phase value and the most significant bit of the second accumulated phase value are reset when the most significant bit of both said first accumulated phase value and said second accumulated phase value are simultaneously 1.

22. A method according to claim 21, wherein two equal bits are reset whenever these bits are 1 at the same time.

23. A phase comparator for carrying out the method in accordance to claim 13-22, wherein the first signal is a reference signal and the second signal is an input signal, said phase comparator including:

a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in said reference signal,

a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in said input signal, and

means or arithmetic means for determining the phase error based on the second accumulated phase value and the first accumulated phase value.

24. A phase comparator according to claim 23, wherein the arithmetic means comprises subtracting means for determining the phase error by subtracting the second accumulated phase value from the first accumulated phase value.

25. A phase comparator according to claim 23 or 24, wherein the phase comparator includes a digital-to-analogue converter adapted to convert the phase error and thereby to generate an analogue output signal.

26. A phase comparator according to any one of the claims 23-25, wherein the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for

generating a first analogue representation of said first logic bit by bit AND operation, and

means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND operation.

27. A phase comparator according to claim 26, wherein the converter circuit comprises current mode logic circuits giving a current output for a two bit AND operation, said current output being used for generating an analogue representation for a bit by bit AND operation.

28. A phase comparator according to claim 26 or 27, wherein the arithmetic means are adapted to obtain one or more analogue phase error signals based on the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

29. A phase comparator according to claim 28, wherein the arithmetic means comprises subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the first analogue representation.

30. A phase comparator according to claim 23 or 24, wherein the phase comparator includes a first and a second digital-to-analogue converter adapted to convert the first and the second accumulated phase value and thereby to generate analogue representations thereof, and that the subtracting means are adapted to perform an analogue subtraction of the analogue representation of said second accumulated phase value from the analogue representation of said first accumulated phase value.

31. A phase comparator according to claim 30, wherein the phase comparator includes a first and a second AND-means, where the output of said first AND-means is connected to a first digital-to-analogue converter, whereby a first accumulator is connected to a first non-inverting input of said first AND-means, and whereby a second accumu-lator is connected to a first inverting input of said first AND-means,

the output of said second AND-means being connected to said second digital-to-analogue converter, and that said second accumulator further is connected to a first non-inverting input of said second AND-means, said first accumulator further being connected to a first inverting input of said second AND-means.

32. A phase comparator according to any one of the claims 23-31, wherein the phase comparator includes a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

33. A converter circuit for obtaining an analogue presentation of a digital input signal or of a logical operation on several digital input signals, at least one of the digital input signals having at least 2 bits, said circuit comprising

a number of current mode logic circuits, CML circuits arranged in modules, with each CML circuit having one or more logic input signals, a first current line, a second current line and a constant current source, each of said CML circuits further comprising means for switching the constant current source between a first conductive state, in which the current source draws or delivers current via the first current line, and a second conductive state, in which the current source draws or delivers current via the second current line, said switching being controlled by at least one of the logic input signals, wherein

a first module has at least one CML circuit, with each CML circuit of the first module having a first logic input signal representing the first bit value of a first digital input signal and providing a first control signal for the switching between the first and the second conductive state, and

a second module has at least one CML circuit, with each CML circuit of the second module having a first logic input signal representing the second bit value of the first digital input signal and providing a first control signal for the switching between the first and the second conductive state.

34. A converter circuit according to claim 33, wherein the first digital signal has N-bits, and wherein for each bit k, where k is selected as an integer larger than or equal to zero and smaller than or equal to N-1, there is a corresponding module k having at least one CML circuit, with each CML circuit of the module k having a first logic input signal representing the value of the corresponding bit k of the first digital input signal and providing a first control signal for the switching between the first and the second conductive state.

35. A converter circuit according to claim 33 or 34, wherein the current drawn from or delivered to said first current lines of the CML circuits arranged in the modules is used for generating a first analogue output for the converter circuit.

36. A converter circuit according to any one of the claims 33-35, wherein at least part or all of the CML circuits have said logic input signals together with the inverse of said logic input signals as input signals for controlling the switching between the first and the second conductive state.

37. A converter according to any one of the claims 34-36, wherein for each module k, there is one corresponding CML circuit.

38. A converter circuit according to claims 35 and 37, wherein the current drawn from or supplied to the first lines of the CML circuits of the modules is used for generating the first analogue output as a voltage output via a first resistor network or via a first capacitor network.

39. A converter according to any one of the claims 34-36, wherein for each module k, there are 2^k corresponding CML circuits.

40. A converter circuit according to claims 35 and 37, wherein the sum of the current drawn from or supplied to the first lines of the CML circuits of the modules is used for generating the first analogue output as a current output.

41. A converter circuit according to any one of the claims 33-40, wherein for the first module, the logic of each CML circuit is designed so that in order for the first logic input signal to control the state of a CML circuit to be in the first conductive state, the first bit of the first digital signal shall be active.

42. A converter circuit according to any one of the claims 33-41, wherein for the second module, the logic of each CML circuit is designed so that in order for the first logic input signal to control the state of a CML circuit to be in the first conductive state, the second bit of the first digital signal shall be active.

43. A converter circuit according to any one of the claims 34-42, wherein for module k, the logic of each CML circuit is designed so that in order for the first logic input signal to control the state of a CML circuit to be in the first conductive state, the corresponding bit k of the first digital signal shall be active.

44. A converter circuit according to any one of the claims 33-43, wherein a part or all of the CML circuits of said modules are designed as buffer or inverter circuits having only one logic input signal together with the inverse of said logic signal, said logic signal representing a corresponding bit of the first digital signal.

45. A converter circuit according to any one of the claims 33-43, said converter circuit being designed for obtaining an analogue presentation of a bit by bit logic operation of the first digital signal and a second digital signal, said first and second digital signals having the same number of bits, wherein the CML circuits having a first logic input signal representing the value of a corresponding bit of the first digital signal are designed as first logic operating circuits, each said first logic operating circuit further having as input signal a second logic input signal representing a value of a corresponding bit of the second digital signal, and said second logic input signal providing a second control signal for the switching between the first and the second conductive state.

46. A converter circuit according to claim 45, wherein each first logic operating circuit is designed for performing a logic operation selected between the following logic operations: AND, NAND, OR, NOR, XOR or XNOR.

47. A converter circuit according to claim 45 or 46, wherein said first logic operating CML circuits also have as input signals the inverse signals of the first and second logic input signals.

48. A converter circuit according to any one of the claims 45-47, wherein the logic of said first logic operating circuits is designed as first AND operating circuits, said AND operating circuits being designed so that in order for the first and second logic input signals to control the state of a CML circuit to be in the first conductive state, the corresponding bit values of the first digital signal and the second digital signal shall both be active.

49. A converter circuit according to claim 48, wherein said switching means of a first AND operating CML circuit comprises a first switch being controlled by the first logic signal, a second switch being controlled by the inverse of the first logic signal, a third switch being controlled by the second logic signal, and a fourth switch being controlled by the inverse of the second logic signal.

50. A converter circuit according to claim 49, wherein said switches are arranged so that the CML circuit is in the first conductive state drawing or delivering current via the first current line through the first and third switches when the bit values corresponding to the first and second logic signals are both active, and

so that the CML circuit is in the second conductive state drawing or delivering current via the second current line through the second and the third switches when the bit value corresponding to the first logic signal is non-active and the bit value corresponding to the second logic signal is active, or through the fourth switch when the bit values corresponding to the first and second logic signals are both non-active.

51. A converter circuit according to any one of the claims 45-50, wherein the first and second logic signals being input to the same first logic operating CML circuit correspond to the same bit number of the first and the second digital signal, respectively.

52. A converter circuit according to any one of the claims 45-51, said converter circuit further being designed for obtaining an analogue presentation of a bit by bit logic operation on a third and a fourth digital signal, said third and fourth digital signals having the same number of bits and having at least 2 bits.

53. A converter circuit according to claim 52, wherein the first, second, third and fourth digital signals have the same number of bits.

54. A converter circuit according to claims 52 or 53, said converter circuit further comprising a number of CML circuits being designed as second logic operating circuits, with each second logic operating circuit having at least a first logic input signal representing the value of a corresponding bit of the third digital signal and a second logic input signal representing the value of a corresponding bit of the fourth digital signal, a third current line, a fourth current line and a constant current source, each of said second logic operating circuits further comprising means for switching the constant current source between a first conductive state, in which the current source draws or delivers current via the third current line, and a second conductive state, in which the current source draws or delivers current via the fourth current line, said switching being controlled by at least said first and second logic input signals.

55. A converter circuit according to claim 54, wherein the current drawn from or delivered to the first current lines of the first logic operating circuits arranged in the modules is used for generating a first analogue output for the converter circuit, and wherein the current drawn from or delivered to the third current lines of the second logic operating circuits arranged in the modules is used for generating a second analogue output for the converter circuit.

56. A converter circuit according to claim 54 or 55, wherein each second logic operating circuit is designed as a logic operating circuit selected between the following logic operating circuits: AND, NAND, OR, NOR, XOR or XNOR logic operating circuit.

57. A converter circuit according to any one of the claims 54-56, wherein the first and the second logic operating circuits are both designed for performing the same logic operation.

58. A converter circuit according to any one of the claims 54-57, wherein said second logic operating CML circuits also have as input signals the inverse signals of the first and second logic input signals.

59. A converter circuit according to any one of the claims 54-58, wherein the second logic operating circuits are designed as second AND operating circuits, to thereby obtain an analogue presentation of a bit by bit AND operation on the third and the fourth digital signals.

60. A converter circuit according to claim 59, wherein the third and fourth digital signals have P-bits, and wherein for each bit m, where m is selected as an integer larger than or equal to zero and smaller than or equal to P-1, there is a corresponding module m having at least one second AND operating circuit, with each second AND operating circuit of the module m having a first logic input signal representing the value of the corresponding bit m of the third digital signal and providing a first control signal for the switching between the first and the second conductive state, and with each second AND operating circuit of the module m having a second logic input signal representing the value of the corresponding bit m of the fourth digital signal and providing a second control signal for the switching between the first and the second conductive state.

61. A converter circuit according to claim 59 or 60, wherein the logic of said CML circuits being designed as second AND operating circuits is designed so that in order for the first and second logic input signals to control the state of a second AND operating circuit to be in the first conductive state, the corresponding bit values of the third digital signal and the fourth digital signal shall both be active.

62. A converter circuit according to any one of the claims 59-61, wherein said switching means of a second AND operating circuit comprises a first switch being controlled by the first logic signal, a second switch being controlled by the inverse of

the first logic signal, a third switch being controlled by the second logic signal, and a fourth switch being controlled by the inverse of the second logic signal.

63. A converter circuit according to claim 62, wherein said switches are arranged so that the second AND operating circuit is in the first conductive state drawing or delivering current via the third current line through the first and third switches when the bit values corresponding to the first and second logic input signals are both active, and

so that the second AND operating circuit is in the second conductive state drawing or delivering current via the fourth current line through the second and the third switches when the bit value corresponding to the first logic signal is non-active and the bit value corresponding to the second logic signal is active, or through the fourth switch when the bit values corresponding to the first and second logic input signals are both non-active.

64. A converter circuit according to any one of the claims 54-63, wherein the first and second logic signals being input to the same second logic operating circuit correspond to the same bit number of the third and the fourth digital signals, respectively.

65. A converter circuit according to any one of the claims 52-64, wherein said third and fourth digital signals are the inverse signals of the first and second digital signals, respectively, or the inverse signals of the second or first digital signals, respectively.

66. A converter according to claim 37 and any one of the claims 60-65, wherein for each module m, there is one corresponding second logic operating circuit.

67. A converter according to claim 39 and any one of the claims 60-65, wherein for each module m, there are 2^m corresponding second AND operating circuits.

68. A converter circuit according to any one of the claims 33-43, said converter circuit being designed for obtaining an analogue presentation of a bit by bit first logic operation on the first digital signal and a second digital signal, and for obtaining an

analogue presentation of a bit by bit first logic operation of the inverse signals of the first and second digital signals, said first and second digital signals having the same number of bits.

69. A converter circuit according to claim 68, wherein the CML circuits having a first logic input signal representing the value of a corresponding bit of the first digital signal are designed as combined logic operating circuits, each combined logic operating circuit further having:

a second logic input signal representing a value of a corresponding bit of the second digital signal, and a third current line;

said switching means further being adapted for switching the constant current source between the first conductive state, in which the current source draws or delivers current via the first current line, the second conductive state, in which the current source draws or delivers current via the second current line, and a third conductive state in which the current source draws or delivers current via the third current line; and

said first and second logic input signals providing corresponding first and second control signals for the switching between the first, second and third conductive states.

70. A converter circuit for obtaining an analogue presentation of a bit by bit first logic operation on a first digital signal and a second digital signal, and for obtaining an analogue presentation of a bit by bit first logic operation of the inverse signals of the first and second digital signals, said first and second digital signals having the same number of bits, said circuit comprising:

a number of current mode logic circuits, CML circuits, being designed as combined logic operating circuits, with each combined logic operating circuit having a first logic input signal representing the value of a corresponding bit of the first digital signal and a second logic input signal representing a value of a corresponding bit of the second digital signal, a first current line, a second current line, a third current line and a constant current source, each of said combined logic operating circuits further having means for switching the constant current source between a first conductive state, in which the current source draws or delivers current via the first current line, a second conductive state, in which the current source draws or

delivers current via the second current line, and a third conductive state in which the current source draws or delivers current via the third current line; and

said first and second logic input signals providing corresponding first and second control signals for the switching between the first, second and third conductive states.

71. A converter circuit according to claim 69 or 70, wherein the current drawn from or delivered to the first current lines of the combined logic operating circuits arranged in the modules is used for generating a first analogue output for the converter circuit, and wherein the current drawn from or delivered to the third current lines of the combined logic operating circuits arranged in the modules is used for generating a second analogue output for the converter circuit.

72. A converter circuit according to any one of the claims 68-71, wherein the converter circuit is designed so that the first logic operation is selected between the following logic operations: AND, NAND, OR, NOR, XOR or XNOR logic operating circuit.

73. A converter circuit according to any one of the claims 69-72, wherein each combined logic operating circuit is designed as a combined AND operating circuit, to thereby obtain an analogue presentation of a bit by bit AND operation on the first digital signal and the second digital signal, and for obtaining an analogue presentation of a bit by bit AND operation of the inverse signals of the first and second digital signals.

74. A converter circuit according to any one of the claims 69-73, wherein each combined logic operating circuit further has a third logic input signal representing the inverse value of the bit corresponding to the first digital signal, and a fourth logic input signal representing the inverse value of the bit corresponding to the second digital signal, said third and fourth logic input signals providing corresponding third and fourth control signals for the switching between the first, second and third conductive states.

75. A converter circuit according to claim 73 or 74, wherein the logic of the combined AND operating CML circuits is designed so that in order for the logic input signals to control the state of a combined AND operating circuit to be in:

the first conductive state, the corresponding bit values of the first digital signal and the second digital signal shall both be active;

the third conductive state, the corresponding bit values of the first digital signal and the second digital signal shall both be non-active; and

the second conductive state, the corresponding bit value of the first digital signal shall be non-active with the corresponding bit value of the second digital signal being active, or the corresponding bit value of the first digital signal shall be active with the corresponding bit value of the second digital signal being non-active.

76. A converter circuit according to any one of the claims 68-75, wherein the first and second logic input signals corresponds to the same bit number of the first and second digital signals, respectively.

77. A converter circuit according to any one of the claims 73-76, wherein the switching means of the combined AND operating circuit comprises a first switch being controlled by the first logic signal, a second switch being controlled by the third logic signal or the inverse of the first logic signal, a third switch being controlled by the second logic signal, a fourth switch being controlled by the fourth logic signal or the inverse of the second logic signal, a fifth switch being controlled by the third logic signal of the inverse of the first logic signal, and a sixth switch being controlled by the first logic signal.

78. A converter circuit according to claim 77, wherein said switches are arranged so that the combined AND operating circuit is in:

the first conductive state drawing or delivering current via the first current line through the first and third switches when the bit values corresponding to the first and second logic signals are both active;

the third conductive state drawing or delivering current via the third current line through the fifth and fourth switches when the bit values corresponding to the first and second logic signals are both non-active;

the second conductive state drawing or delivering current via the second current line through the third and second switches when the bit value corresponding to the first logic signal is non-active and the bit value corresponding to the second logic signal is active; and

the second conductive state drawing or delivering current via the second current line through the sixth and fourth switches when the bit value corresponding to the first logic signal is active and the bit value corresponding to the second logic signal is non-active.

79. A digital to analogue converter circuit according to any one of the claims 33-78, wherein the number of CML circuits are powered by the same power supply having a positive supply terminal and a negative or ground terminal.

80. A converter circuit according to any one of the claims 33-79, wherein the constant current sources of each of the CML circuits of said modules or each of the CML circuits are designed to draw or deliver substantially the same current.

81. A converter circuit according to any one of the claims 39-80, wherein the converter circuit has modules with CML circuits, and wherein for each module corresponding to bit k there are 2^k corresponding CML circuits having a first current line and a second current line, each said first current line being supplied from the same, first supply line.

82. A converter circuit according to claims 81, wherein the current drawn from or delivered to said first supply line by the first current lines represent a first analogue output signal for the converter circuit.

83. A converter circuit according to any one of the claims 69-80, wherein the converter circuit has modules with combined logic operating CML circuits, and wherein for each module corresponding to bit k there are 2^k corresponding combined logic operating circuits having a first current line, a second current line and a third current line, each said first current line being supplied from the same, first supply line, and each said third current line being supplied from the same, third supply line.

84. A converter circuit according to claims 83, wherein the current drawn from or delivered to said first supply line by the first current lines represent a first analogue output signal for the converter circuit, and the current drawn from or delivered to said third supply line by the third current lines represent a second analogue output signal for the converter circuit.

85. A converter circuit according to any one of the claims 54-82, wherein the converter circuit has modules with second logic operating CML circuits, and wherein for each module corresponding to bit m there are 2^m corresponding CML circuits having a third current line and a fourth current line, each said third current line being supplied from the same, third supply line.

86. A converter circuit according to claims 85, wherein the current drawn from or delivered to said third supply line by the third current lines represent a second analogue output signal for the converter circuit.

87. A converter circuit according to claim 37 and any one of the claims 41-80, wherein the converter circuit has modules with CML circuits, and wherein for each module corresponding to bit k there is one corresponding CML circuit having a first current line and a second current line, each said first current line being supplied from the same power supply via a first resistor network or via a first capacitor network having a first voltage output representing a first analogue output signal for the converter circuit.

88. A converter circuit according to claim 37 and any one of the claims 69-80, wherein the converter circuit has modules with combined logic operating CML circuits, and wherein for each module corresponding to bit k there is one corresponding combined logic operating circuit having a first current line, a second current line and a third current line, each said first current line being supplied from the same power supply via a first resistor network or via a first capacitor network having a first voltage output representing a first analogue output signal for the converter circuit, and each said third current line being supplied from said power supply via a second resistor network or via a second capacitor network having a

second voltage output representing a second analogue output signal for the converter circuit.

89. A converter circuit according to claim 37 and any one of the claims 54-80, wherein the converter circuit has modules with second logic operating CML circuits, and wherein for each module corresponding to bit m there is one corresponding CML circuit having a third current line and a fourth current line, each said third current line being supplied from the same power supply via a second resistor network or via a second capacitor network having a second voltage output representing a second analogue output signal for the converter circuit.

90. A converter circuit according to any one of the claims 87-89, wherein the first resistor network is formed as a first R –2R network having the first voltage output.

91. A converter circuit according to any of the claims 88-90, wherein the second resistor network is formed as a second R –2R network having the second voltage output.

92. A converter circuit according to any one of the claims 79-91, wherein the second current lines of the CML circuits are powered by the positive terminal of the power supply or via a resistor connected to the positive terminal of the power supply.

93. A converter circuit according to any one of the claims 79-92, wherein the converter circuit has second logic operating circuits, and wherein the fourth current lines of the second logic operating CML circuits are powered by the positive terminal of the power supply or via a resistor connected to the positive terminal of the power supply.

94. A converter circuit according to claim 92 and 93, wherein the second current lines and the fourth current lines of the CML circuits are powered from the same supply line.

95. A converter circuit according to any one of the claims 79-94, wherein the constant current sources of the CML circuits are delivering current to the negative or ground terminal of the power supply.

96. A converter according to any one of the claims 33-95, wherein the switching means of the CML circuits is made using N-MOS technology.

97. A converter according to any one of the claims 33-91, wherein the switching means of the CML circuits is made using P-MOS technology.

98. A phase-locked loop according to any one of the claims 6-9, wherein the converter circuit of the phase comparator comprises first AND operating circuits and second AND operating circuits for performing said first and second logic bit by bit operation, respectively, said first and second AND operating circuits being selected from claims 48-51and claims 59-67 or selected from claims 48-51 and 59 and claims 79-82, 85-87, 89-97, and wherein the output of the first accumulator is the first digital signal, the inverted output of the second accumulator is the second digital signal, the inverted output of the first accumulator is the third digital signal, and the output of the second accumulator is the fourth digital signal.

99. A phase-locked loop according to any one of the claims 6-9, wherein the converter circuit of the phase comparator comprises combined AND operating circuits for performing said first and second logic bit by bit operation, said combined AND operating circuits being selected from claims 73-78 or selected from claim 73 and claims 79-84, 88, 90-92, 95-97, and wherein the output of the first accumulator is the first digital signal, and the inverted output of the second accumulator is the second digital signal.